Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

1. (Currently Amended) A multiple integrated circuit control system, comprising:

a multiple integrated circuit controller configured to initiate and control data transactions between the multiple integrated circuit controller and integrated circuits;

a data link configured to communicate the data transactions between the multiple integrated circuit controller and one or more of the integrated circuits, the multiple integrated circuit controller including a first push-pull driver to drive the data transactions; ~~and~~

a non-arbitrated clock signal link configured to communicate a continuous timing clock signal generated by only the multiple integrated circuit controller to the integrated circuits, the multiple integrated circuit controller including a second push-pull driver to drive the clock signal.

2. (Original) A multiple integrated circuit control system as recited in claim 1, wherein the data link and the clock signal link form a two-wire control data bus.

3. (Original) A multiple integrated circuit control system as recited in claim 1, wherein the data link is further configured to communicate write data from the multiple integrated circuit controller to one or more of the integrated circuits.

4. (Original) A multiple integrated circuit control system as recited in claim 1, wherein the data link is further configured to communicate read data from one or more of the integrated circuit to the multiple integrated circuit controller.

5. (Original) A multiple integrated circuit control system as recited in claim 1, wherein the multiple integrated circuit controller is further configured to control a write data transaction from the multiple integrated circuit controller to a first integrated circuit via the data link, and control a read data transaction from a second integrated circuit to the multiple integrated circuit controller via the data link.

6. (Original) A multiple integrated circuit control system as recited in claim 1, wherein the clock signal link is further configured to communicate a continuous clock signal generated by the multiple integrated circuit controller to one or more of the integrated circuits.

7. (Original) A multiple integrated circuit control system as recited in claim 1, wherein the clock signal link is further configured to communicate a pulsed clock signal generated by the multiple integrated circuit controller to one or more of the integrated circuits.

8. (Original) A multiple integrated circuit control system as recited in claim 1, wherein the data link is further configured to communicate error check data between the multiple integrated circuit controller and one or more of the integrated circuits.

9. (Original) A multiple integrated circuit control system as recited in claim 1, wherein:

the multiple integrated circuit controller is further configured to communicate a unique target identifier via the data link to initiate a data transaction with an integrated circuit that has an address identified by the unique target identifier;

in an event that the data transaction is a write data transaction, the data link is further configured to communicate the data from the multiple integrated circuit controller to the identified integrated circuit; and

in an event that the data transaction is a read data transaction, the data link is further configured to communicate the data from the identified integrated circuit to the multiple integrated circuit controller.

10. (Previously Presented) A printing device comprising the multiple integrated circuit control system as recited in claim 1 wherein the multiple integrated circuit control executes computer executable instructions initiated from a processor of the printing device.

11. (Currently Amended) A multiple integrated circuit control, comprising:

a clock signal output configured to communicate a continuously timing clock signal generated by only the multiple integrated circuit controller to integrated circuits via a non-arbitrated first data link of a data bus;

a first push-pull driver configured to drive the clock signal on the first data link;

a data input / output configured to communicate data between the multiple integrated circuit control and one or more of the integrated circuits via a second data link of the data bus; and

a second push-pull driver configured to drive the data on the second data link.

12. (Original) A multiple integrated circuit control as recited in claim 11 implemented as a single-ended interface control circuit.

13. (Currently Amended) A multiple integrated circuit control as recited in claim 11 implemented as a low voltage differential signalling interface control circuit.

14. (Currently Amended) A multiple integrated circuit control as recited in claim 11 implemented as a low voltage differential signalling interface control circuit, wherein:

the first data link is a differential clock signal link configured to communicate the clock signal as a low voltage differential clock signal; and

the second data link is a differential data link configured to communicate the data as a low voltage differential data signal.

15. (Original) A multiple integrated circuit control as recited in claim 11, wherein the data input / output is further configured to communicate write data from the multiple integrated circuit control to an integrated circuit via the second data link.

16. (Original) A multiple integrated circuit control as recited in claim 11, wherein the data input / output is further configured to communicate read data from an integrated circuit to the multiple integrated circuit control via the second data link.

17. (Original) A multiple integrated circuit control as recited in claim 11, wherein the data input / output is further configured to communicate write data from the multiple integrated circuit control to a first integrated circuit, and communicate read data from a second integrated circuit to the multiple integrated circuit control.

18. (Original) A multiple integrated circuit control as recited in claim 11, wherein the clock signal output is further configured to communicate a continuous clock signal generated by the multiple integrated circuit control to the integrated circuits via the first data link.

19. (Original) A multiple integrated circuit control as recited in claim 11, wherein the clock signal output is further configured to communicate a pulsed clock signal generated by the multiple integrated circuit control to the integrated circuits via the first data link.

20. (Original) A multiple integrated circuit control as recited in claim 11, wherein the data input / output is further configured to communicate error check data between the multiple integrated circuit control and one or more of the integrated circuits via the second data link.

21. (Original) A multiple integrated circuit control as recited in claim 11, wherein:

the data input / output is further configured to communicate a unique target identifier via the second data link to initiate a data transaction with an integrated circuit that has an address identified by the unique target identifier;

in an event that the data transaction is a write data transaction, the data input / output is further configured to communicate the data from the multiple integrated circuit control to the identified integrated circuit; and

in an event that the data transaction is a read data transaction, the data input / output is further configured to communicate the data from the identified integrated circuit to the multiple integrated circuit control.

22. (Previously Presented) A printing device comprising the multiple integrated circuit control as recited in claim 11 wherein the multiple integrated circuit control executes computer executable instructions initiated from a processor of the printing device.

23. (Previously Presented) An application-specific integrated circuit (ASIC) configured with the multiple integrated circuit control as recited in claim 11 wherein the multiple integrated circuit control of the ASIC includes logic to control the integrated circuits.

24. (Currently Amended) A method, comprising:

communicating a continuously timing clock signal generated from only a multiple integrated circuit control to integrated circuits via a non-arbitrated first data link, the clock signal being driven with a first push-pull driver of the multiple integrated circuit control; and

communicating data between the multiple integrated circuit control and one or more of the integrated circuits via a second data link, the data being driven with a second push-pull driver of the multiple integrated circuit control.

25. (Original) A method as recited in claim 24, wherein:

communicating the clock signal includes communicating the clock signal as a low voltage differential clock signal; and

communicating the data includes communicating the data as a low voltage differential data signal.

26. (Original) A method as recited in claim 24, wherein communicating the data includes communicating write data from the multiple integrated circuit control to an integrated circuit via the second data link.

27. (Original) A method as recited in claim 24, wherein communicating the data includes communicating read data from an integrated circuit to the multiple integrated circuit control via the second data link.

28. (Original) A method as recited in claim 24, further comprising:

controlling a write data transaction from the multiple integrated circuit control to a first integrated circuit via the second data link; and

controlling a read data transaction from a second integrated circuit to the multiple integrated circuit control via the second data link.

29. (Original) A method as recited in claim 24, wherein communicating the clock signal includes communicating a continuous clock signal from the multiple integrated circuit control to the integrated circuits.

30. (Original) A method as recited in claim 24, wherein communicating the clock signal includes communicating a pulsed clock signal from the multiple integrated circuit control to the integrated circuits.

31. (Original) A method as recited in claim 24, further comprising communicating error check data between the multiple integrated circuit control and an integrated circuit via the second data bus link.

32. (Original) A method as recited in claim 24, further comprising communicating a unique target identifier via the second data link to initiate a data transaction with an integrated circuit that has an address identified by the unique target identifier.

33. (Original) A method as recited in claim 24, further comprising communicating a unique target identifier via the second data link to initiate a data transaction with an integrated circuit that has an address identified by the unique target identifier, wherein:

in an event that the data transaction is a write data transaction, communicating the data includes communicating the data from the multiple integrated circuit control to the identified integrated circuit; and

in an event that the data transaction is a read data transaction, communicating the data includes communicating the data from the identified integrated circuit to the multiple integrated circuit control.

34. (Original) A single-ended interface control circuit comprising a multiple integrated circuit control configured to perform the method as recited in claim 24.

35. (Currently Amended) A low voltage differential signalling interface control circuit comprising a multiple integrated circuit control configured to perform the method as recited in claim 24.

36. (Previously Presented) A method as recited in claim 24, wherein communicating the data via the second data link includes:

communicating a data transaction start indication from the multiple integrated circuit control to the integrated circuits;

communicating a unique target identifier to initiate the data transaction with an integrated circuit that is identified by the unique target identifier;

communicating control data from the multiple integrated circuit control to define the data transaction with the identified integrated circuit;

communicating a control parity bit from the multiple integrated circuit control to the integrated circuit having the unique target identifier for control data error checking at the identified integrated circuit;

communicating the data between the multiple integrated circuit control and the identified integrated circuit, wherein the multiple integrated circuit control is a data sending device and the identified integrated circuit is a data receiving device in an event that the data is communicated from the multiple integrated circuit control to the identified integrated circuit, further wherein the multiple integrated circuit control is the data receiving device and the identified integrated circuit is the data sending device in an event that the data is communicated from the identified integrated circuit to the multiple integrated circuit control;

communicating a data parity bit for data error checking at the data receiving device;

communicating a data acknowledgement from the data receiving device to the data sending device to indicate receipt of the data and the data parity bit; and

communicating a data transaction stop indication from the data sending device to the data receiving device to indicate receipt of the data acknowledgement.

37. (Currently Amended) Computer-readable media comprising computer executable instructions that, when executed, direct a multiple integrated circuit control to:

communicate a continuously timing clock signal generated from only the multiple integrated circuit control to integrated circuits via a non-arbitrated first data link of a data bus, the clock signal being driven by a first push-pull driver of the multiple integrated circuit control;

communicate write data from the multiple integrated circuit control to an integrated circuit via a second data link of the data bus according to a write data transaction initiated by the multiple integrated circuit control, the write data being driven by a second push-pull driver of the multiple integrated circuit control; and

communicate read data from the integrated circuit to the multiple integrated circuit control via the second data link of the data bus according to a read data transaction initiated by the multiple integrated circuit control.

38. (Previously Presented) Computer-readable media as recited in claim 37, further comprising computer executable instructions that, when executed, direct the multiple integrated circuit control to coordinate the write data transaction and the read data transaction via the second data link of the data bus.

39. (Previously Presented) Computer-readable media as recited in claim 37, further comprising computer executable instructions that, when executed, direct the multiple integrated circuit control to communicate the clock signal as a continuous clock signal generated by the multiple integrated circuit control to the integrated circuits.

40. (Previously Presented) Computer-readable media as recited in claim 37, further comprising computer executable instructions that, when executed, direct the multiple

integrated circuit control to communicate the clock signal as a pulsed clock signal generated by the multiple integrated circuit control to the integrated circuits.

41. (Previously Presented) Computer-readable media as recited in claim 37, further comprising computer executable instructions that, when executed, direct the multiple integrated circuit control to communicate error check data between the multiple integrated circuit control and one or more of the integrated circuits via the second data link.

42. (Previously Presented) Computer-readable media as recited in claim 37, further comprising computer executable instructions that, when executed, direct the multiple integrated circuit control to communicate a unique target identifier via the second data link to initiate a data transaction with an integrated circuit that has an address identified by the unique target identifier.

43. (Currently Amended) A multiple integrated circuit control, comprising:

means to communicate a continuously timing clock signal driven only by a first push-pull driver to integrated circuits via a non-arbitrated first data link of a data bus;

means to initiate and communicate write data driven by a second push-pull driver to an integrated circuit via a second data link of the data bus; and

means to initiate and receive read data from the integrated circuit via the second data link of the data bus.

44. (Original) A multiple integrated circuit control as recited in claim 43, further comprising means to coordinate a write data transaction to communicate the write data to the integrated circuit and a read data transaction to receive the read data from the integrated circuit.

45. (Original) A multiple integrated circuit control as recited in claim 43, further comprising means to generate the clock signal as a continuous clock signal.

46. (Original) A multiple integrated circuit control as recited in claim 43, further comprising means to generate the clock signal as a pulsed clock signal.

47. (Original) A multiple integrated circuit control as recited in claim 43, further comprising means to error check data communications between the multiple integrated circuit control and one or more of the integrated circuits.

48. (Original) A multiple integrated circuit control as recited in claim 43, further comprising means to communicate a unique target identifier via the second data link to initiate a data transaction with an integrated circuit that has an address identified by the unique target identifier.